
Zero-Drift, Rail-to-Rail I/O CMOS Operational Amplifiers

Features

- **Low Offset Voltage: 20 μ V**
- **Input Offset Drift: 0.05 μ V/ $^{\circ}$ C**
- **Gain Bandwidth Product: 15KHz**
- **Rail-to-Rail Input and Output**
- **High Gain, CMRR, PSRR:110dB**
- **Slew Rate: 10V/ms**
- **Low Power Consumption: 25 μ A (TYP RS8504)**
- **Overload Recovery Time:150us**
- **Low Supply Voltage: +2.5 V to +5.5 V**
- **No External Capacitors Required**
- **Extended Temperature: -40 $^{\circ}$ C to +125 $^{\circ}$ C**

Applications

- **Temperature Sensors**
- **Medical/Industrial Instrumentation**
- **Pressure Sensors**
- **Battery-Powered Instrumentation**
- **Active Filtering**
- **Weight Scale Sensor**
- **Strain Gage Amplifiers**
- **Power Converter/Inverter**

Description

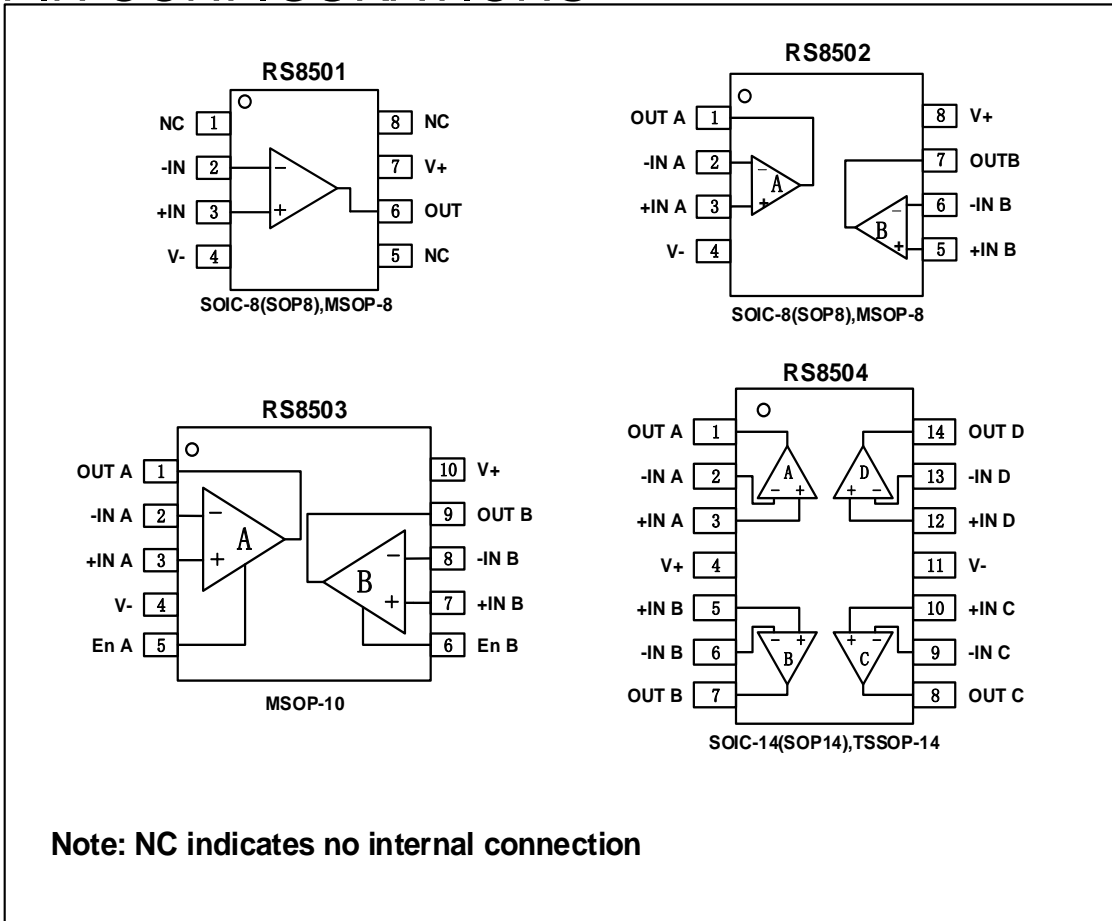
The RS8501,RS8502,RS8504,RS8503(dual version &shutdown)series of CMOS operational amplifiers use auto-zero techniques to simultaneously provide very low offset voltage (200 μ V max) and near-zero drift over time and temperature. This family of amplifiers has ultralow noise, offset and power.

This miniature, high-precision operational amplifiers offset high input impedance and rail-to-rail input and rail-to-rail output swing. With high gain-bandwidth product of 15KHz and slew rate of 10V/ms.

Single or dual supplies as low as +2.5V(\pm 1.25V) and up to +5.5V (\pm 2.75V) may be used.

The RS8501/RS8502/RS8504/RS8503(dual version with shutdown) are specified for the extended industrial and automotive temperature range (-40 $^{\circ}$ C to 125 $^{\circ}$ C). The RS8501 single amplifier is available in 8-lead MSOP8 and 8-lead SOIC packages, The RS8502 dual amplifier is available in 8-lead SOIC and 8-lead TSSOP narrow surface mount packages, The RS8503(dual version with shutdown) comes in *Micro-SIZE* MSOP-10. The RS8504 quad is available in 14-lead SOIC and 14-lead narrow TSSOP packages.

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Supply Voltage, V+ to V-.....	7.0V
Input Terminals, Voltage ⁽²⁾	- 0.5 to (V+) + 0.5V
Current ⁽²⁾	±10mA
Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +125°C
Junction Temperature.....	150°C
Package Thermal Resistance @ T _A = +25°C	
SOT23-5, SOT23-6.....	200°C/W
MSOP-10, SOIC-8	150°C/W
SOIC-14, TSSOP-14.....	100°C/W
Lead Temperature (Soldering, 10s)	260°C
ESD Susceptibility	
HBM	5000V
MM	400V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.



ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	ORDERING NUMBER	TEMPRANGE	PACKAGE	PACKAGE MARKING	TRANSPORT MEDIA, QUANTITY
RS8501	RS8501XK	-40°C~125°C	SOIC-8(SOP8)	RS8501	Reel,2500
RS8501	RS8501XM	-40°C~125°C	MSOP-8	RS8501	Reel,3000
RS8502	RS8502XK	-40°C~125°C	SOIC-8(SOP8)	RS8502	Reel,2500
RS8502	RS8502XM	-40°C~125°C	MSOP-8	RS8502	Reel,3000
RS8503	RS8502XN	-40°C~125°C	MSOP-10	RS8503	Reel,3000
RS8504	RS8504XP	-40°C~125°C	SOIC-14(SOP14)	RS8504	Reel,2500
RS8504	RS8504XQ	-40°C~125°C	TSSOP-14	RS8504	Reel,3000

ELECTRICAL CHARACTERISTICS

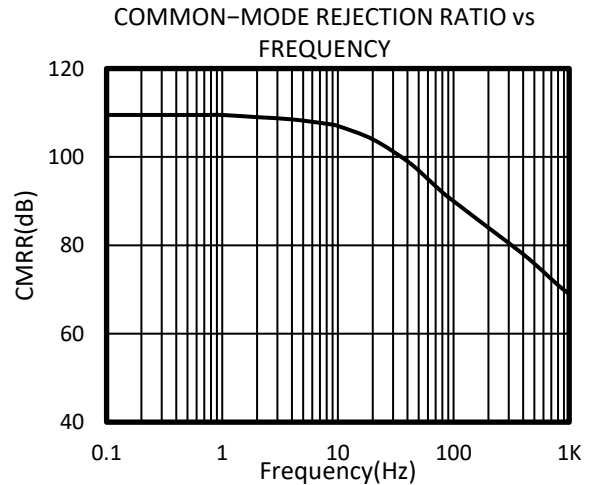
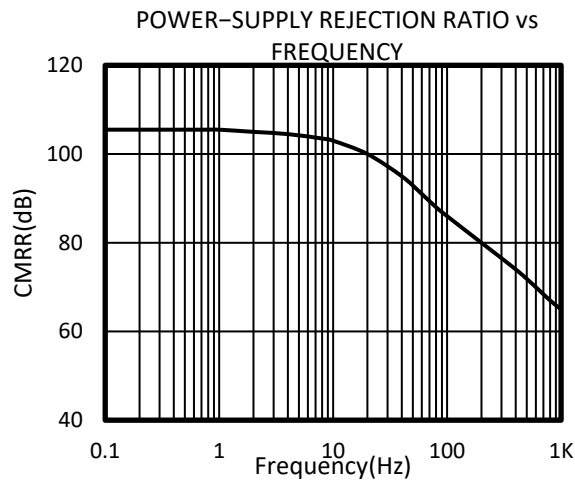
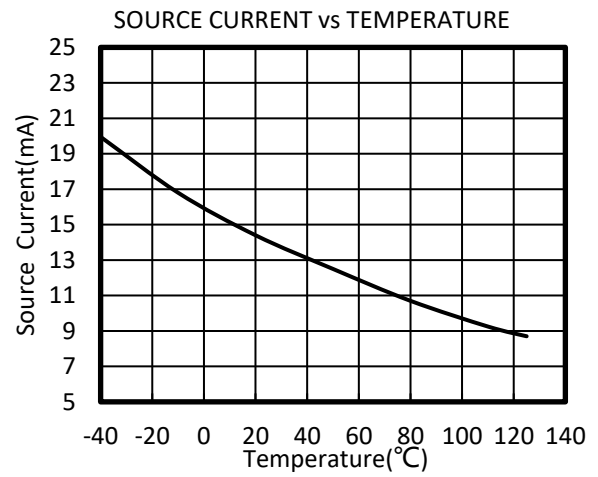
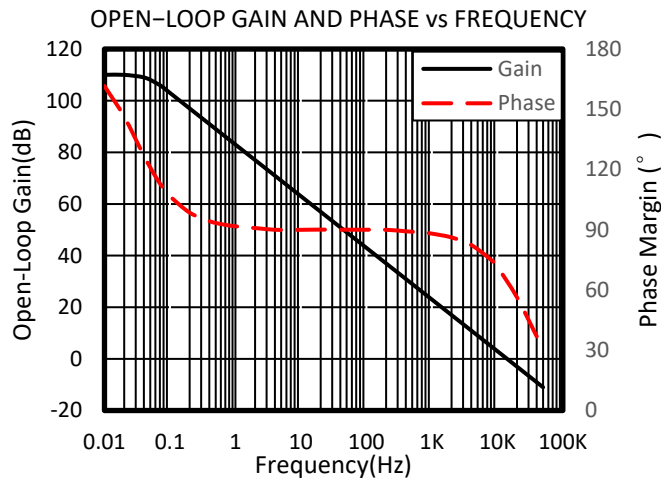
Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$.

(At $T_A = +25^{\circ}\text{C}$, $V_S=5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{\text{OUT}} = V_S/2$, unless otherwise noted.)

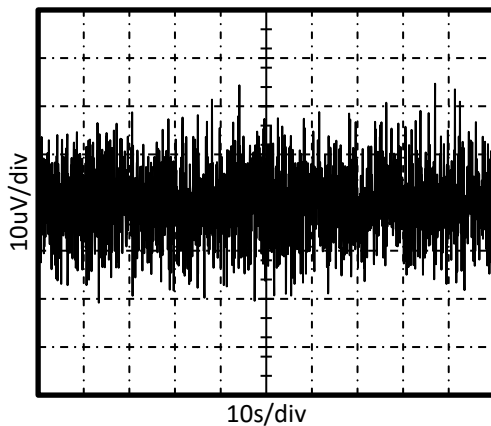
PARAMETER	CONDITION	RS8501, RS8502, RS8503, RS8504			UNIT
		MIN	TYP	MAX	
OFFSET VOLTAGE					
Input Offset Voltage V_{OS}	$V_{\text{CM}} = V_S/2$		20	200	μV
VS Temperature dV_{OS}/dT			0.05	0.30	$\mu\text{V}/^{\circ}\text{C}$
VS Power Supply PSRR	$V_S = +2.5\text{V}$ to $+5.5\text{V}$, $V_{\text{CM}} = 0$	100	110		dB
Channel Separation, dc			0.1		$\mu\text{V}/\text{V}$
INPUT BIAS CURRENT					
Input Bias Current I_B	$V_{\text{CM}} = V_S/2$		5		pA
Input Offset Current I_{OS}			5		pA
NOISE PERFORMANCE					
Input Voltage Noise $e_{\text{n,p-p}}$	$f=0.01\text{Hz}$ to 10Hz		25		μV_{pp}
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range V_{CM}		(V-)-0.1		(V+)+0.1	V
Common-Mode Rejection Ratio CMRR	$(V-) - 0.1\text{V} < V_{\text{CM}} < (V+) + 0.1\text{V}$	100	110		dB
INPUT CAPACITANCE					
Differential			1		pF
Common-Mode			5		pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain A_{OL}	$R_L=10\text{K}\Omega$, $V_O=0.3\text{V}$ to 4.7V, -40°C~125°C	100	110		dB
DYNAMIC PERFORMANCE					
Slew Rate SR	$G=+1$		10		V/ms
Gain-Bandwidth Product GBW			15		KHz
Overload Recovery Time			150		us
OUTPUT CHARACTERISTICS					
Output Voltage High V_{OH}	$R_L=100\text{K}\Omega$ to GND	4.99	4.998		V
	$R_L=10\text{K}\Omega$ to GND	4.95	4.98		V
Output Voltage Low V_{OL}	$R_L=100\text{K}\Omega$ to V+		1	10	mV
	$R_L=10\text{K}\Omega$ to V+		10	30	mV
Short-Circuit Current I_{SC}			14		mA
POWER SUOOLY					
Operating Voltage Range		2.5		5.5	V
Quiescent Current I_Q	RS8504, $V_S=5\text{V}$		25		μA
Quiescent Current I_Q	RS8504, $V_S=3.3\text{V}$		20		μA
SHUTDOWN					
t_{OFF}			2		μs
t_{ON}			1		ms
V_L (shutdown)		0		+0.8	V
V_H (amplifier is active)		0.75(V+)		V+	V
Input Bias Current of Enable Pin			50		pA
I_{QSD}			1	5	μA

TYPICAL CHARACTERISTICS

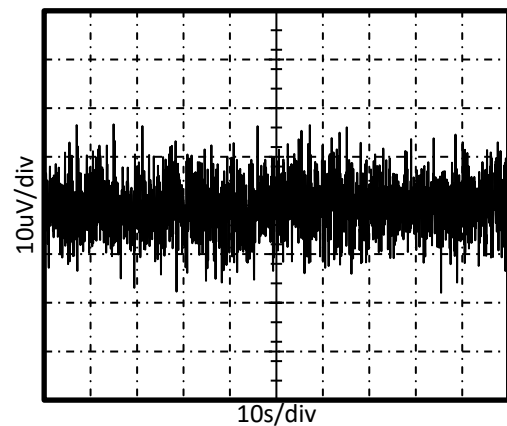
At $T_A = +25^\circ\text{C}$, $V_S = 5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, $V_{OUT} = V_S/2$, unless otherwise noted.



0.01Hz TO 10Hz NOISE AT $V_S = 5\text{V}$

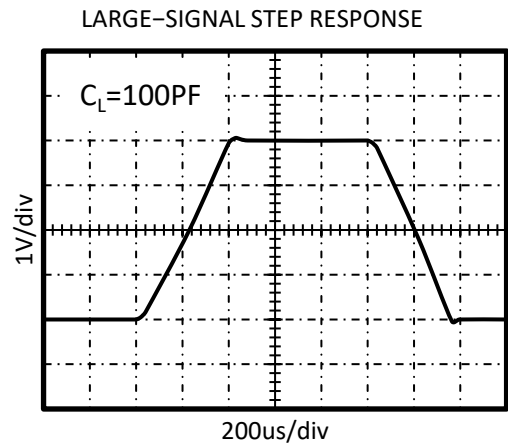
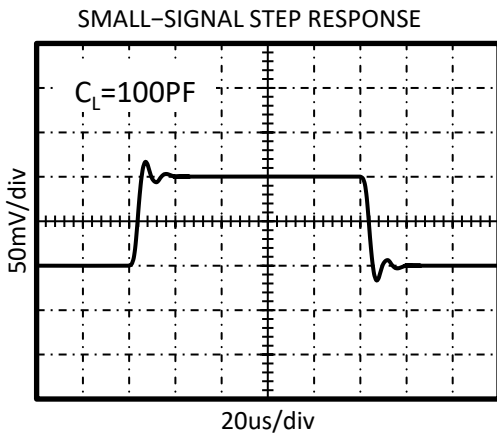
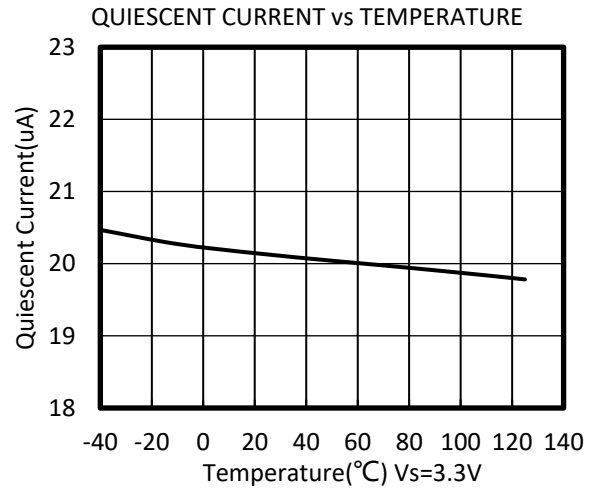
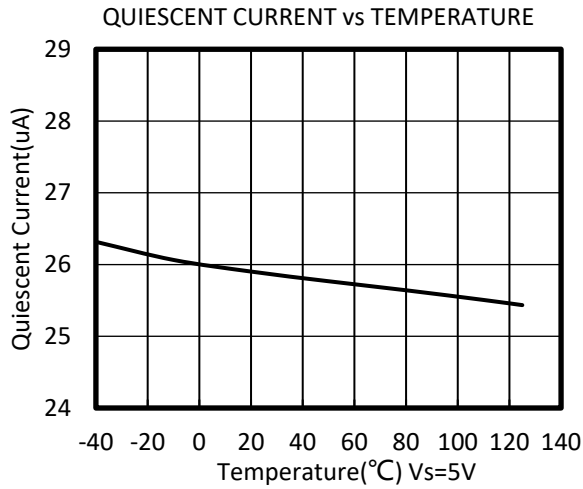


0.01Hz TO 10Hz NOISE AT $V_S = 3.3\text{V}$



TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_S = 5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, $V_{OUT} = V_S/2$, unless otherwise noted.



APPLICATION NOTES

The RS8501, RS8502, RS8503, RS8504 series op amps are unity-gain stable and free from unexpected output phase reversal. They use auto-zeroing techniques to provide low offset voltage and very low drift over time and temperature.

Good layout practice mandates use of a 0.1 μ F capacitor placed closely across the supply pins.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring that they are equal on both input terminals.

- Use low thermoelectric-coefficient connections (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat-sources.
- Shield op amp and input circuitry from air currents, such as cooling fans.

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1 μ V/ $^{\circ}$ C or higher, depending on materials used.

OPERATING VOLTAGE

The RS8501, RS8502, RS8503, RS8504 series op amps operate over a power-supply range of +2.5V to +5.5V (± 1.25 V to ± 2.75 V). Supply voltages higher than 7V (absolute maximum) can permanently damage the amplifier. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

RS8503 ENABLE FUNCTION

The enable/shutdown digital input is referenced to the V $_{-}$ supply voltage of the amp. A logic high enables the op amp. A valid logic high is defined as >

75% of the total supply voltage. The valid logic high signal can be up to 5.5V above the negative supply, independent of the positive supply voltage. A valid logic low is defined as < 0.8V above the V $_{-}$ supply pin. If dual or split power supplies are used, be sure that logic input signals are properly referred to the negative supply voltage. The Enable pin must be connected to a valid high or low voltage, or driven, not left open circuit.

The logic input is a high-impedance CMOS input, with separate logic inputs provided on the dual version. For battery operated applications, this feature can be used to greatly reduce the average current and extend battery life.

The enable time includes one full autozero cycle required by the amplifier to return to V $_{OS}$ accuracy. Prior to this time, the amplifier functions properly, but with unspecified offset voltage.

Disable time is 1 μ s. When disabled, the output assumes a high-impedance state. This allows the RS8503 to be operated as a gated amplifier, or to have the output multiplexed onto a common analog output bus.

LAYOUT GUIDELINES

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1 μ F capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the EMI (electromagnetic-interference) susceptibility.

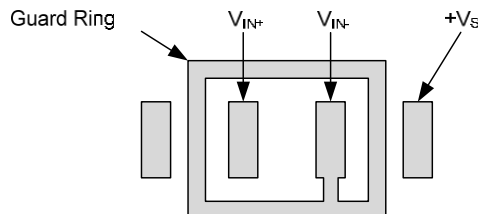
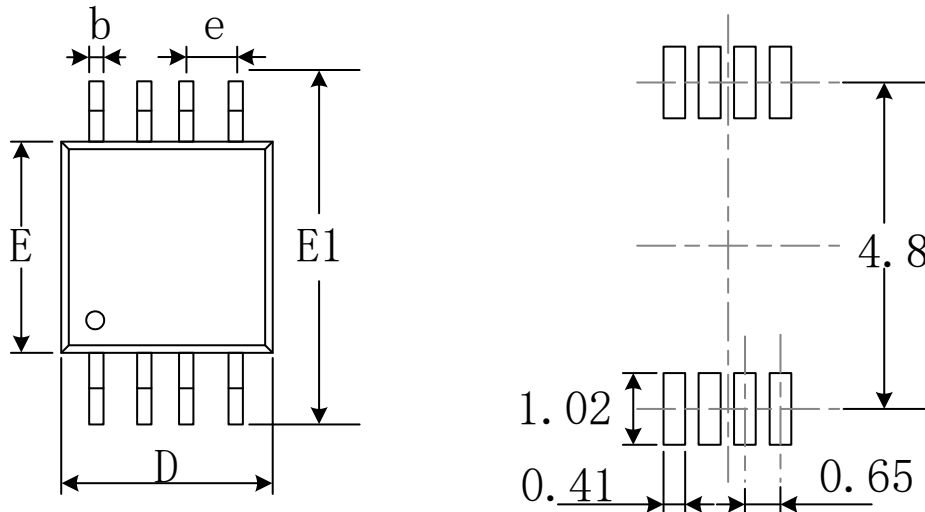
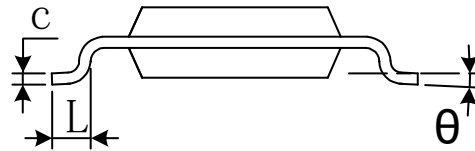
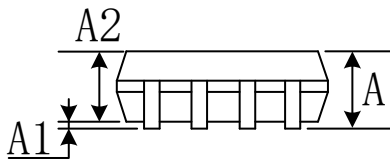


Figure 1. The Layout of Guard Ring

PACKAGE OUTLINE DIMENSIONS MSOP-8

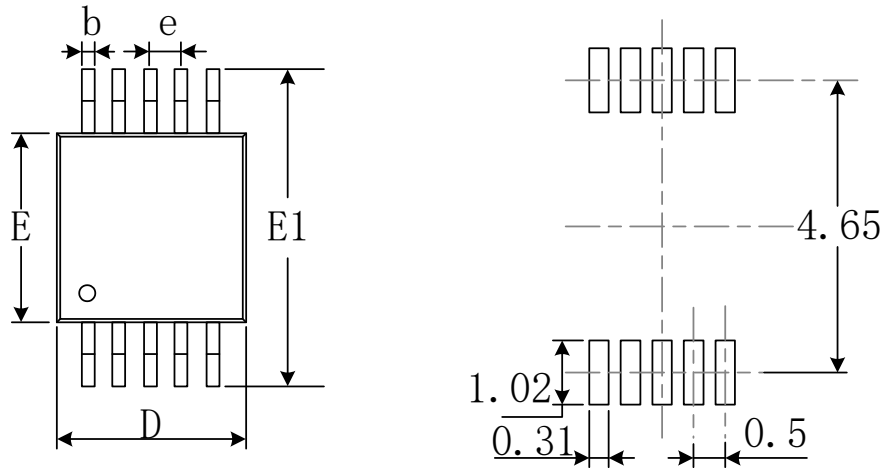


RECOMMENDED LAND PATTERN (Unit: mm)

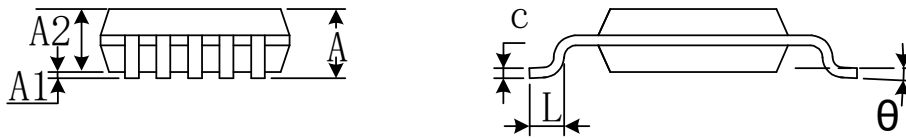


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.650(BSC)		0.026(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

MSOP-10

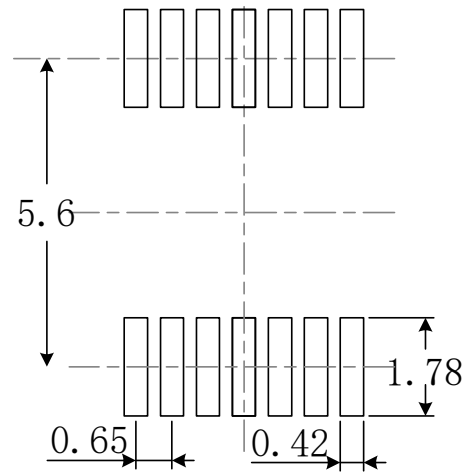
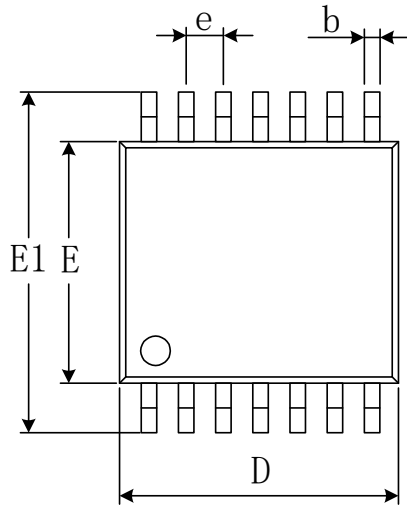


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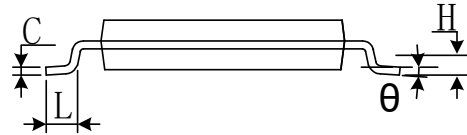
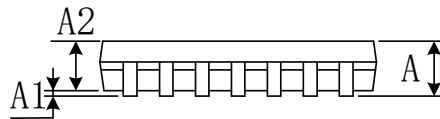


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.50(BSC)		0.020(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

TSSOP-14

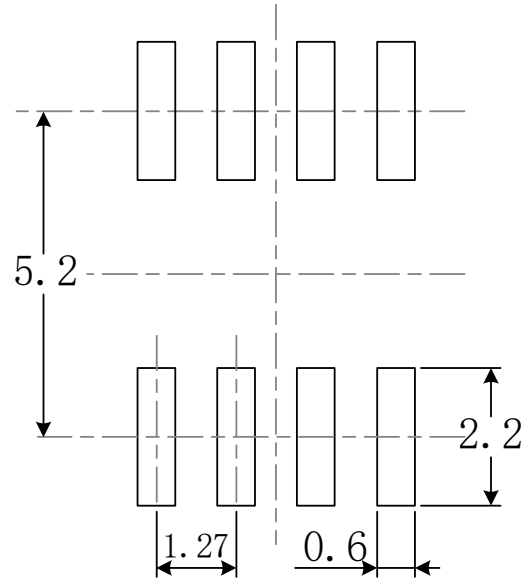
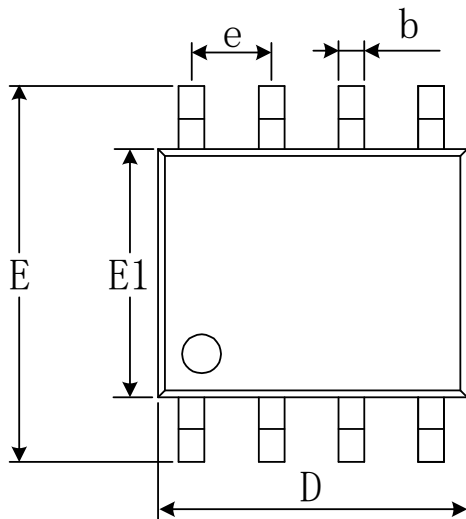


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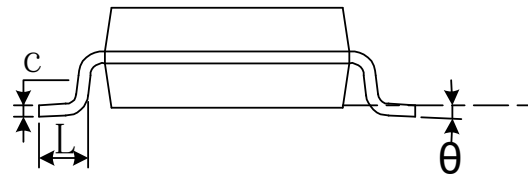
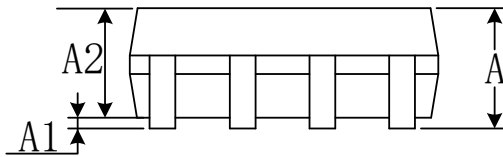


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.860	5.100	0.191	0.201
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

SOIC-8(SOP8)

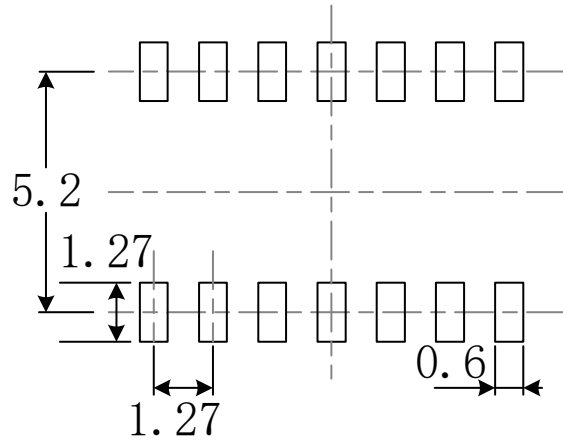
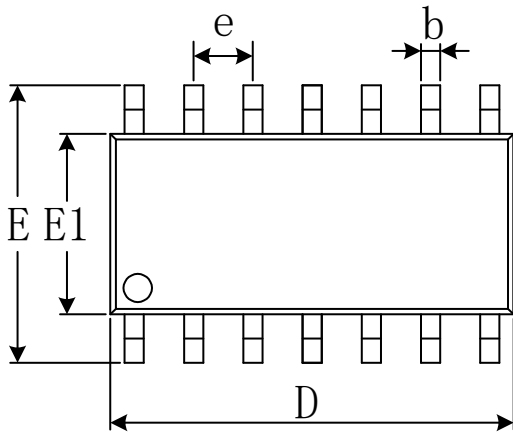


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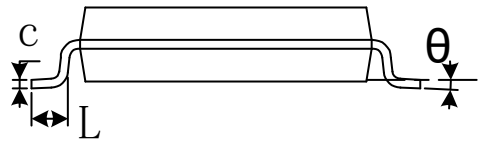
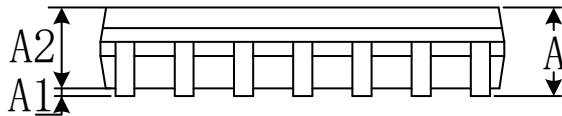


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270(BSC)		0.050(BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

SOIC-14(SOP14)



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
e	1.270(BSC)		0.050(BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°